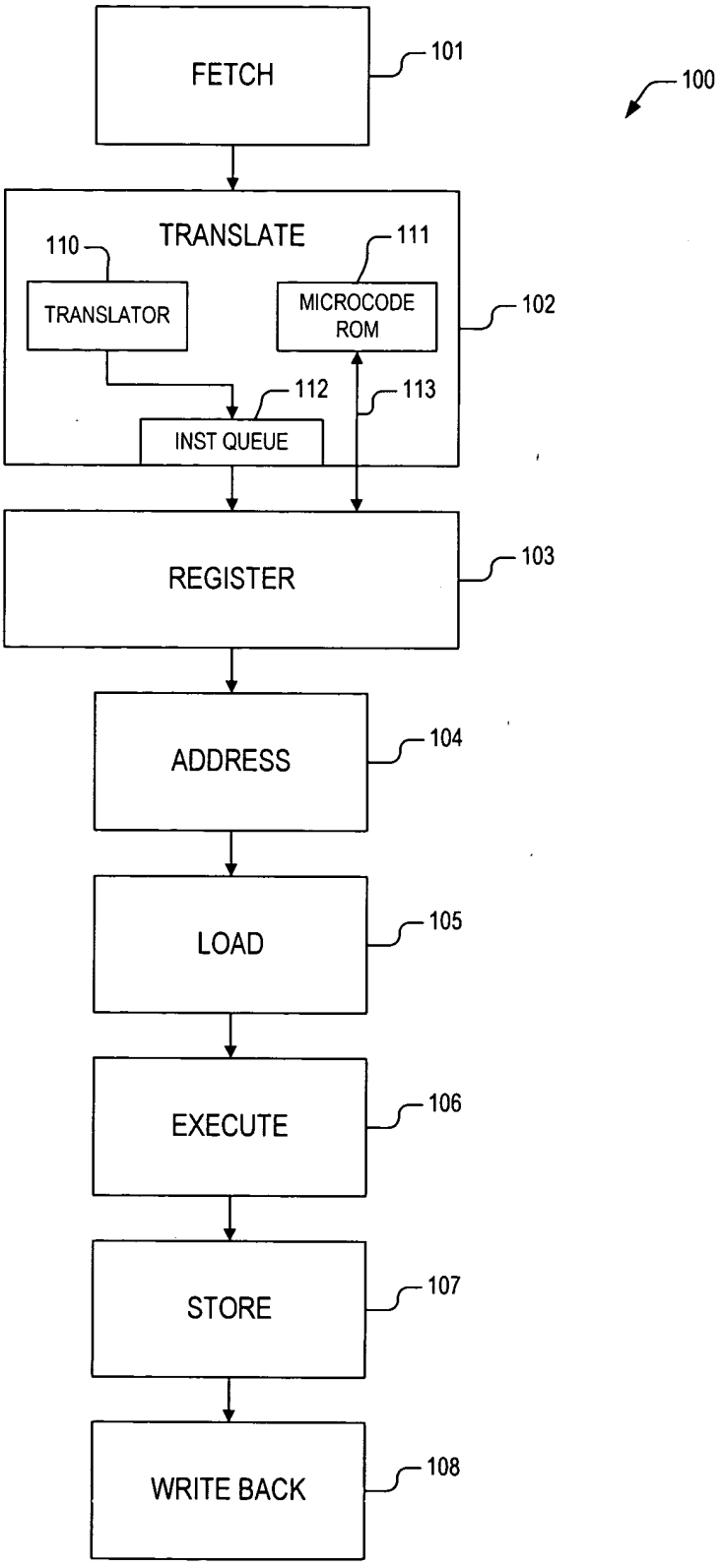
FETCH
101
100
TRANSLATE
110
111
TRANSLATOR
MICROCODE ROM
102
112
113
INST QUEUE
REGISTER
103
ADDRESS
104
LOAD
105
EXECUTE
106
STORE
107
WRITE BACK
108

FIG. 1

200

CYCLE	TRANSLATE	REGISTER	ADDRESS
1	INST_1	---	---
2	INST_2	MIC_1.1	---
3	INST_3	MIC_2.1, MEP_2	MIC_1.1
4	---	MIC_2.2	MIC_2.1
5	---	MIC_2.3	MIC_2.2
6	---	***	MIC2.3
7	---	MIC_2.4	***
8	---	MIC_2.5	MIC_2.4
9	---	MIC_3.1	MIC_2.5
10	---	---	MIC_3.1

ROM ACCESS DELAY

FIG. 2

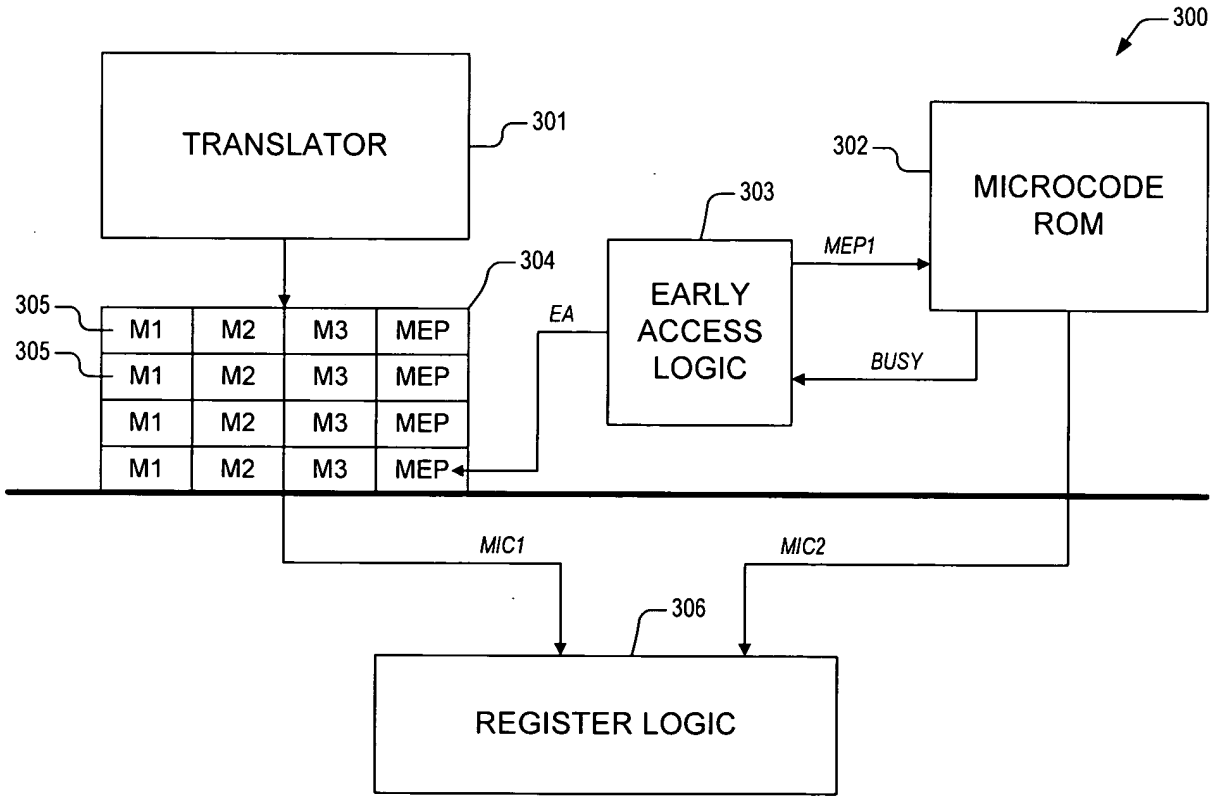

FIG. 3

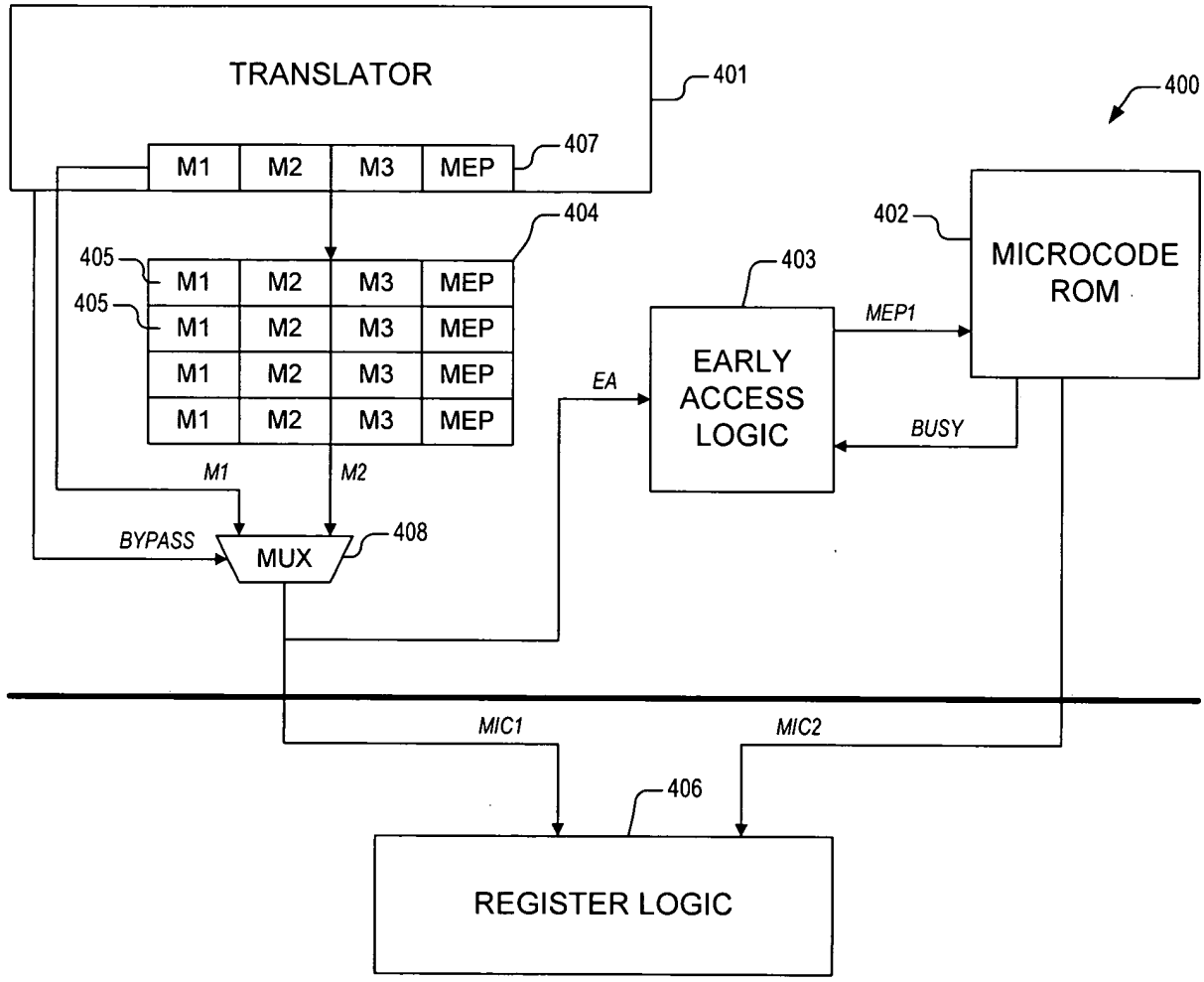
TRANSLATOR
401
400
M1
M2
M3
MEP
407
404
405
405
M1
M2
M3
MEP
M1
M2
M3
MEP
M1
M2
M3
MEP
402
MICROCODE ROM
403
EARLY ACCESS LOGIC
MEP1
EA
BUSY
M1
M2
BYPASS
MUX
408
MIC1
MIC2
406
REGISTER LOGIC

FIG. 4

CYCLE	TRANSLATE	REGISTER	ADDRESS
1	INST_1	---	---
2	INST_2	MIC_1.1	---
3	INST_3	MIC_2.1, MEP_2	MIC_1.1
4	---	MIC_2.2	MIC_2.1
5	---	MIC_2.3	MIC_2.2
6	---	MIC_2.4	MIC2.3
7	---	MIC_2.5	MIC_2.4
8	---	MIC_3.1	MIC_2.5
9	---	---	MIC_3.1

500

ROM ACCESS DELAY

FIG. 5